

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-68. (Canceled).

69. (Currently Amended) An integrated circuit comprising:

one or more wells of a first conductivity type;

one or more wells of a second conductivity type;

a first plurality of transistors within said one or more wells of a first conductivity type;

a second plurality of transistors within said one or more wells of a second conductivity type;

a deep well of a second conductivity type disposed between said one or more wells of said first conductivity type and a substrate of said first conductivity type, wherein said deep well includes a plurality of substructures having a plurality of gaps between each of said one or more wells of said first conductivity type and said substrate of said first conductivity type, wherein said one or more wells of said first conductivity type are coupled to said substrate through said plurality of gaps, and wherein said substructures form a depletion region between said deep well and said substrate having a specified amount of decoupling capacitance for a principal operating

potential coupled between said deep well and said substrate; and

a separation well of said first conductivity type disposed within one or more of said gaps and coupling said one or more wells of said first conductivity type to said substrate, ~~wherein a doping concentration of said separation well is greater than said one or more wells of said first conductivity type and said substrate.~~

70. (Canceled).

71. (Currently Amended) The integrated circuit of Claim 69, wherein said deep well is further coupled to said one or more wells of said second conductivity type and disposed between said one or more wells of said second conductivity type and said substrate, ~~and wherein said deep well further includes a plurality of substructures having a second plurality of gaps wherein said one or more wells of said second conductivity type are adjacent to said substrate.~~

72. (Canceled).

73. (Previously Presented) The integrated circuit of Claim 69, further comprising:
one or more additional wells of said first conductivity type;

one or more additional wells of said second conductivity type; and

a second deep well of said second conductivity type disposed between said one or more additional wells of said first and second conductivity type and said substrate, wherein said one or more additional wells of said first conductivity type are isolated from said substrate by said second deep well.

74. (Withdrawn – Currently Amended) The integrated circuit of Claim 69, further comprising:

one or more additional wells of said first conductivity type;

one or more additional wells of said second conductivity type;

a second deep well of said second conductivity type disposed between said one or more additional wells of said first and second conductivity type and said substrate, wherein said one or more additional wells of said first conductivity type are isolated from said substrate by said second deep well;

a third deep well of said second conductivity type disposed beneath said first and second deep wells and substantially surrounded by said substrate, wherein said third deep well includes a plurality of substructures having said substrate disposed within ~~said~~ gaps between said plurality of substructures of said third deep well, and wherein said substructures of said third deep well form a depletion region between said third deep well and said substrate to provide an additional specified amount of decoupling capacitance for said principal operation potential; and

an interlayer well of said second conductivity type coupling said deep well to said third deep well.

75. (New) The integrated circuit of Claim 69, wherein said separation well prevents said gaps from closing under bias conditions.

76. (New) The integrated circuit of Claim 69, wherein said separation well increases said decoupling capacitance between said first and second voltages.

77. (New) An integrated circuit comprising:
a substrate of a first conductivity type;
an epitaxial layer of a first conductivity type disposed on said substrate;
a first surface well of a second conductivity type coupled to a first voltage;
a second surface well of said first conductivity type coupled to a second voltage; and
a first deep well of said second conductivity type coupled to said first voltage by said first surface well, wherein said first deep well is disposed between said second surface well and said epitaxial layer, wherein said first deep well includes a plurality of sub-structures including a plurality of gaps, wherein said gaps provide connectivity between said second surface well and said epitaxial layer, and wherein a depletion region formed between said first deep well and said

surrounding second surface well and epitaxial layer provides a decoupling capacitance between said first and second voltages.

78. (New) The integrated circuit of Claim 77, wherein said first deep well capacitor has a surface area selected to provide a specified amount of decoupling capacitance.

79. (New) The integrated circuit of Claim 77, wherein the width of said gaps do not close under bias conditions.

80. (New) The integrated circuit of Claim 77, further comprising a separation well of said first conductivity type disposed in one or more of said gaps between said sub-structures, wherein said separation well increases said decoupling capacitance between said first and second voltages.

81. (New) The integrated circuit of Claim 77, further comprising a separation well of said first conductivity type disposed in one or more of said gaps between said sub-structures, wherein said separation well reduces said separation required between said substructures such that said gaps between said depletion region does not close under bias conditions.

82. (New) The integrated circuit of Claim 77, wherein said sub-structures of said first deep well comprise substantially parallel stripes.

83. (New) The integrated circuit of Claim 77, wherein said sub-structures of said first deep well comprise a grid.

84. (New) The integrated circuit of Claim 77, further comprising:
a third surface well of said second conductivity type coupled to a third voltage; and
a fourth surface well of said first conductivity type coupled to a forth voltage, wherein said fourth surface well is isolated from said epitaxial layer by said third surface well, an additional deep well of said second conductivity type, and an additional surface well of said second conductivity type.

85. (New – Withdrawn) The integrated circuit of Claim 77, further comprising:
a second deep well of said second conductivity type, wherein said second deep well is disposed in said epitaxial layer, wherein said second deep well includes a plurality of sub-structures that form a depletion region between said second deep well and said surrounding epitaxial layer to provide additional decoupling capacitance between said first and second voltages; and

an implant of said second conductivity type for coupling said second deep well to said first voltage by said first deep well and said first surface well.

86. (New – Withdrawn) The integrated circuit of Claim 85, wherein said first and second deep wells are formed with said same process mask.